The Semiconductor Test Challenge

Seeking Value and High Returns in Semiconductor Test

The complexities and uncertainties associated with the manufacturing of semiconductor devices requires that some level of testing be performed on each device before being put in the latest mobile phone, computer, or automobile. Test is therefore a significant component of a semiconductor product's value stack - enabling design verification, fabrication and packaging process improvement, product configuration, and quality assurance. The semiconductor industry confirms this value by spending an average of about 3.5% of revenue on test, or about US$10 billion annually.

The extent of testing can range from sample testing for devices deploying straightforward designs and mature manufacturing processes, to several stages of lengthy, fully-functional, multi-temperature testing for devices using the latest technologies. The role of test in the semiconductor manufacturing process is shown in the graphic below.

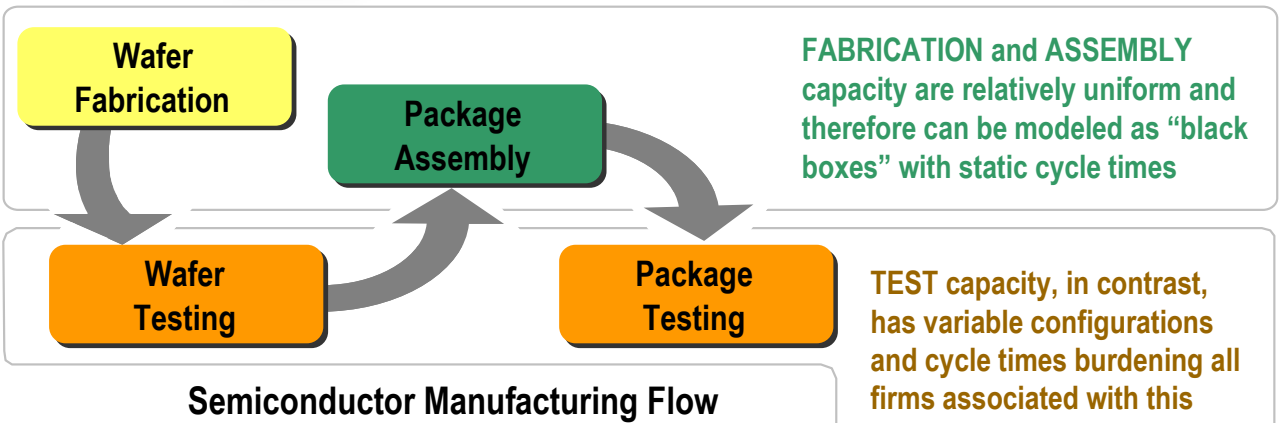
The automatic test equipment (ATE) used to perform the tests on semiconductor devices provide the stimulus to the device, as well as capture and process the response from the device, all under computer control. Since these tools must be able to source and capture many channels of the latest high-speed, high-power, and high-precision signals, the ATE business model requires significant investments in research and development, applications engineering, and other support functions. The current industry average selling price for ATE is therefore in the range of $US0.5 million to $US1.5 million.

Teradyne's UltraFLEX™ Test System

In order to manage the overall cost of test, each tool is typically configured to have only the channels and capability needed to test a particular device, making the manufacturing capacity provided by that test tool dedicated to a given device, or at best, a device family. Each device also has a unique list of required tests, making the cycle time through the test process device-dependent. The test capacity in place today is therefore very diverse and non-uniform, unlike the capacity for the other major steps in the semiconductor manufacturing process shown below.

This variability makes it difficult for test providers to optimize the utilization of costly test assets and thus maximize their return on investment – reducing the economic profits of not only the test provider, but also that of the test specifier and test equipment supplier. The typically-cited one-third of test capacity that is unutilized accounts for an estimated US$1.8 billion of annual depreciation costs, a significant economic burden on the entire semiconductor test value chain.

To begin addressing these semiconductor test challenges, a solution that first and foremost makes transparent the complexities of test capacity is necessary. Such a solution will enable not only optimized planning, but also efficient specification, matching, and trading of test capacity. Only then will the much sought after value and high returns from semiconductor test be realized.



Semiconductor Manufacturing Flow

Chip Nexus™